# EDA322/ DIT798: Digital Design
# Re-Exam - August 2024

Date: August 29, 2024

Time: **14:00-18:00**

Examiner: Ioannis Sourdis

Department: Computer Science and Engineering

Inquiries:
- visit the exam hall during the 1st and 3rd hour,
- contact through phone, phone extension 1744

Duration: 4 hours

Grading scale: 100 points in total

U: 0%-49%,
3: 50%-64%,
4: 65%-84%,
5: 85%-100%

Available references: an A4 paper sheet (2 pages) with student notes, and a calculator are allowed.

General: Submit your solutions, in English, on blank paper sheets. Write legibly; feel free to use figures to get your point across.

The order of answering the questions does not matter (start with the easiest ones).

Please start the solutions for each problem on a new sheet. Please number the sheets so that the solutions are in numerical order.

Note that it is possible to receive partial credit for an answer even if it is not 100% correct.

Your personal identity code is required on each submitted sheet!

Good luck!

**Question 1** Arithmetic: (10 points)
Design a digital circuit composed of multiple Full Adders (FAs), which performs the following computation:

$$Output = A * 9.45$$

*i.e., output is equal to variable A multiplied by the constant 9.5 (9 point 5)*

where A is a 4-bit unsigned number.

How many FAs does the circuit use?

Note: you can use the FA as a black box without showing its gate-level drawing.

**Question 2** Memory: (10 points)
Use memory 1Kbyte blocks that have 1-Byte per entry, to construct a 16Kbyte memory, which has 4-Bytes per entry.
Draw the block diagram of the memory and show how the address bits are connected.

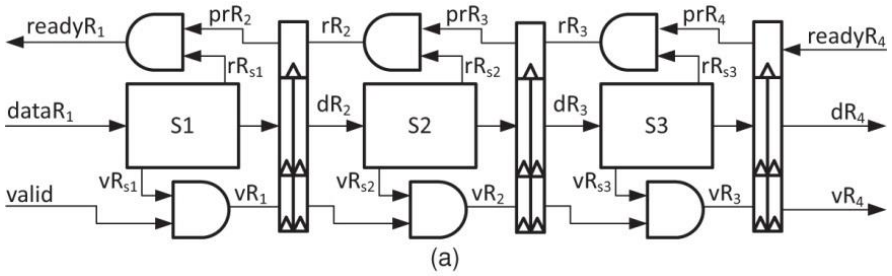
**Question 3** Hazards and Timing: (10 points)

- Minimize the function in the K-map
- Find and remove all hazards.
- What is the latency of the function in its 2 above forms ((i) minimal with hazards and (ii) hazard free ) when the delay of a 2-input AND or OR gate is equal to 1 ns.

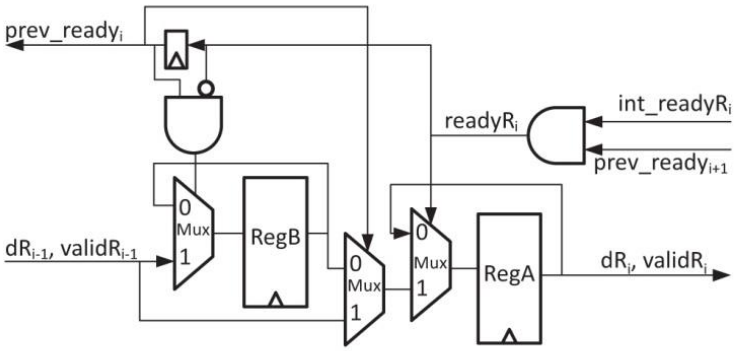
| $x_3x_4$ \ $x_1x_2$ | 00 | 01 | 11 | 10 |
|---|---|---|---|---|
| 00 | | | | |
| 01 | 1 | 1 | 1 | |
| 11 | | | 1 | |
| 10 | 1 | 1 | 1 | |

**Question 4** Number representation: (10 points)
Suppose you need to represent temperature from -20 to + 40 degrees Celsius (C) with a maximum absolute error of 10%. Find a fixed point representation with minimum number of bits that fits the above specification.

**Question 5** Pipelining: (10 points)
Consider the pipeline of the stages shown in Figure (a) bellow, which uses double buffering to support stalling. Each stage has the double buffering circuit of Figure (b) with two registers, RegA and RegB. The first stage of the pipeline receives a new problem (P_i, where i=1, 2, 3 etc.) every cycle S1 is not stalled.



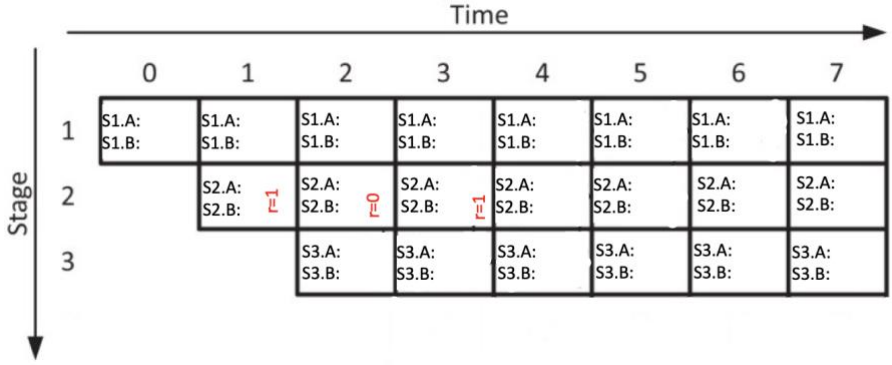
(a)



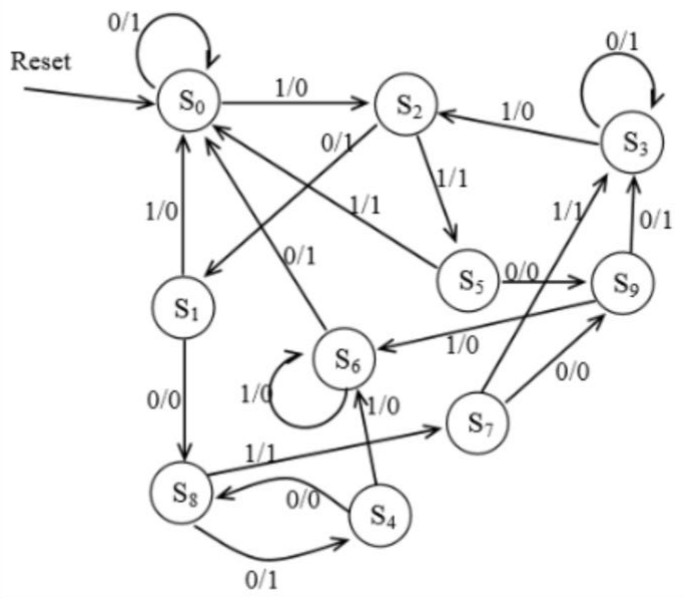
(b)

Fill in the following timing diagram to show the contents of RegA and RegB registers of each stage (S1.A, S1.B, S2.A, S2.B, S3.A, S3.B). The contents of each of these registers can be "Pi" if it stores intermediate results of the problem P_i (e.g. P1, P2, P3, …). Note, that in the beginning the registers are initialized to zero.

Consider that in cycle-0 P_1 enters stage-1. and stage 2 becomes "not ready" (init_readyR2 =0 – denoted as "r=0 in the figure bellow) only in cycle 2. The "Init_readyRi" of all stages are equal to "1" in all other cases.



**Question 6** FSMs: (10 points)
The state diagram defines an FSM with an Input X and an output Z. The values on each arrow in the diagram have the format of X/Z.
a) Minimize the number of states of this FSM and list the equivalent states.
b) Draw the state diagram and state table of the reduced FSM.




**Question 7** Testing: (10 points)
Activate, propagate and justify a stuck-at-0 fault at the carry bit between the 63rd and 64th full adder of a 64-bit ripple carry adder.

**Question 8** Interfaces: (10 points)
Show a full flow control interface between two stages. How would you change the interface to make it (i) a push flow control interface and how would you change it to (ii) a pull flow control interface? What guarantees need pipeline stages to provide in order to support each of the two types of interface (push and pull flow control)?

Which of the three types of interfaces (1. Full flow control, 2. Push flow control, 3. Pull flow control) would be suitable to connect two pipeline stages of:

- a micro-processor
- an adder
- a signal processing unit which takes input from an always-on sensor, e.g., a surveillance camera.

Justify your answer.

**Question 9** Power: (10 points)

1. Describe a metric for measuring energy efficiency of a digital circuit. (2 points)
2. Explain how (i) average and (ii) peak power consumption affect a mobile phone. (4 points)
3. Explain when a digital circuit has dynamic power cost and describe the formula that defines it. What would you do to reduce it? (4 points)

**Question 10** Reconfigurable Computing: (10 points)
Consider the implementation of the following function:

$$F = A_0A_2A_3 + A_1A_2\bar{A}_3 + \bar{A}_0\bar{A}_1\bar{A}_2$$

in 3 different FPGAs, each composed of logic cells with either (i) 5-input LUTs, (ii) 4-input LUTs, or (iii) 3-input LUTs.

a) Show the mapping of the logic of function F in each of the 3 types of FPGAs. How many LUTs are needed in each case? How many bits of SRAM memory are needed in total for each case?

b) Which is the most efficient choice of LUT size in terms of area? What happens to the delay of the function implementation in each case?

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END of EXAM